What is claimed is:

1. A digital signal processing circuit comprising:

a chain of processing units to receive indications of discrete input values, each processing unit being associated with one of a group of filter coefficients; and

a tap selection circuit to select a group of the processing units of the chain to produce an indication of a filtered discrete output value for each discrete input value.

2. The processing unit of claim 1, wherein the chain of processing units comprises a systolic chain.

3. The processing circuit of claim 1, wherein the tap selection circuit selects a number of taps of the processing circuit.

4. The processing circuit of claim 1, wherein the group of processing units progressively accumulate a summed value to form each output value and the tap selection circuit comprises:

a multiplexer to designate a point in the chain at which the accumulation begins.

5. The processing circuit of claim 4, wherein each processing circuit comprises a first input terminal to receive the indications of the discrete input values from a processing circuit input line common to the processing circuits and a second input terminal to receive the indications of the discrete input values from another processing circuit, the multiplexer coupling the first and second terminals of one of the processing circuits together to designate the point in the chain at which the accumulation begins.

6. The processing circuit of claim 1, wherein each processing circuit comprises:

a first adder circuit to generate an indication of a summation of two of the discrete input values; and

a multiplier circuit coupled to the first adder circuit to generate an indication of a product of a coefficient associated with said each processing circuit and the summation of the two discrete values.

7. The processing circuit of claim 6, further comprising:

a second adder circuit coupled to the first multiplier circuit to combine the summation of the two discrete input values with a progressive summation provided by another processing circuit.

8. The processing circuit of claim 7, wherein the tap selection circuit comprises:

a multiplexer to selectively furnish an indication of a zero to the second adder circuit of one of the processing units to designate a point where the progressive sum begins.

9. The processing circuit of claim 1, wherein the tap selection circuit comprises:

a register storing bits indicative of the processing units in the group.

10. The processing circuit of claim 1, wherein each processing unit comprises:

a register storing the indication of the associated filter coefficient.

11. The processing circuit of claim 1, wherein the processing circuit comprises a finite impulse response filter.

12. The processing circuit of claim 1, wherein the processing circuit comprises an infinite impulse response filter.

13. A digital signal processing circuit comprising:

a processing chain having a selectable number of taps; and

a tap selection circuit coupled to the processing chain to selectively establish the number of taps of the chain.

14. The processing circuit of claim 13, wherein the tap selection circuit comprises:

a multiplexer to select one of the taps as the beginning tap in the chain.

15. The processing circuit of claim 14, wherein the multiplexer sets a cumulative sum at the selected tap to zero.

16. The processing circuit of claim 14, wherein the multiplexer sets a delay at the selected tap to zero.

17. The processing circuit of claim 13, wherein the tap selection circuit comprises:

a register storing bits indicative of the number of taps.

18. The processing circuit of claim 13, wherein the tapped delay line comprises:

registers storing indications of filter coefficients associated with the taps.

19. The processing circuit of claim 13, wherein the processing circuit comprises a finite impulse response filter.

20. The processing circuit of claim 13, wherein the processing circuit comprises an infinite impulse response filter.

21. A method comprising:

providing a processing chain line having a fixed number of taps;

disabling some of the taps of the chain; and

using the remaining taps to establish a finite impulse response filter.

22. The method of claim 21, wherein the disabling comprises: selecting one of the taps as the beginning tap in the delay line.

23. The method of claim 21, wherein the disabling comprises: setting a cumulative sum at one of the taps to zero.

24. The method of claim 21, further comprising: storing bits indicative of the number of remaining taps.

25. The method of claim 21, further comprising: storing rewritable indications of filter coefficients associated with the taps.